STIC Search Report
EIC 2600

STIC Database Tracking Number: 159035

TO: Scott Beliveau
Location: Knox 6A01
Art Unit : 2614
Tuesday, July 19, 2005

Case Serial Number: 09/851841

From: Virgil Tyler (ASRC)
Location: KNX 8B68
EIC 2600
Phone: 571-272-8536

virgil.tyler@uspto.gov

Search Notes

Dear Scott,

Please find attached the search results for 09/851,841. I used the search strategy I emailed to you to edit, which you did by your response. I searched the standard Dialog files, IBM TDBs, IEEE, ProQuest, DTIC, ACM and the Internet.

If you would like a re-focus please let me know.

Thank you

STIC Search Results Feedback Form

EIC 2600

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact*:**

Pamela Reynolds, EIC 2600 Team Leader
571-272-3505, Knox 8B59

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2630*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
  (journal articles, conference proceedings, new product announcements etc.)

- *Relevant prior art **not found:***
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2600 Knox 8B59

Wilson (2)

159035

Access DB# 159035

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name Scott Belieau Examiner #: 79346 Date: 7-12-05

Art Unit: 2614 Phone Number _____ Serial Number: 09 851,841

KNX Location: 6A01 Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elec species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define an terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertir claims, and abstract.

Title of Invention: Systems for Receiving and Processing Digital Data carried by satellite transmission

Inventors (please provide full names): James Lundblad; James Baldwin; Louis Coffin

Earliest Priority Filing Date: 5/9/01 *

For Sequence Searches Only Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.

Looking for a STB or other computing device that utilizes a unified memory architecture ~~which is controlled~~ wherein access to the memory is arbitrated by the CPU of the STB. I have a STB with a UMA, however it has a separate memory controller - motivation to use the CPU as the memory controller would be appreciated.

(amended after patent CPU → separate memory controller → now memory controller in CPU single unified unit) *

****

STAFF USE ONLY	Type of Search		Vendors and cost where applicable	
Searcher: Vi Tyler	Sequence (#)		STN	
Searcher Phone #: X-28536	AA Sequence (#)		Dialog	✓
Searcher Location: Knox 8B68	Structure (#)		Questel/Orbit	
Date Searcher Picked Up: 07/15/05	Bibliographic		Dr.Link	
Date Completed: 07/19/05	Litigation	✓	Lexis/Nexis	
Searcher Prep & Review Time: 40	Fulltext		Sequence Systems	✓
Clerical Prep Time:	Patent Family		WWW/Internet	✓
Online Time: 315	Other		Other (specify)	✓

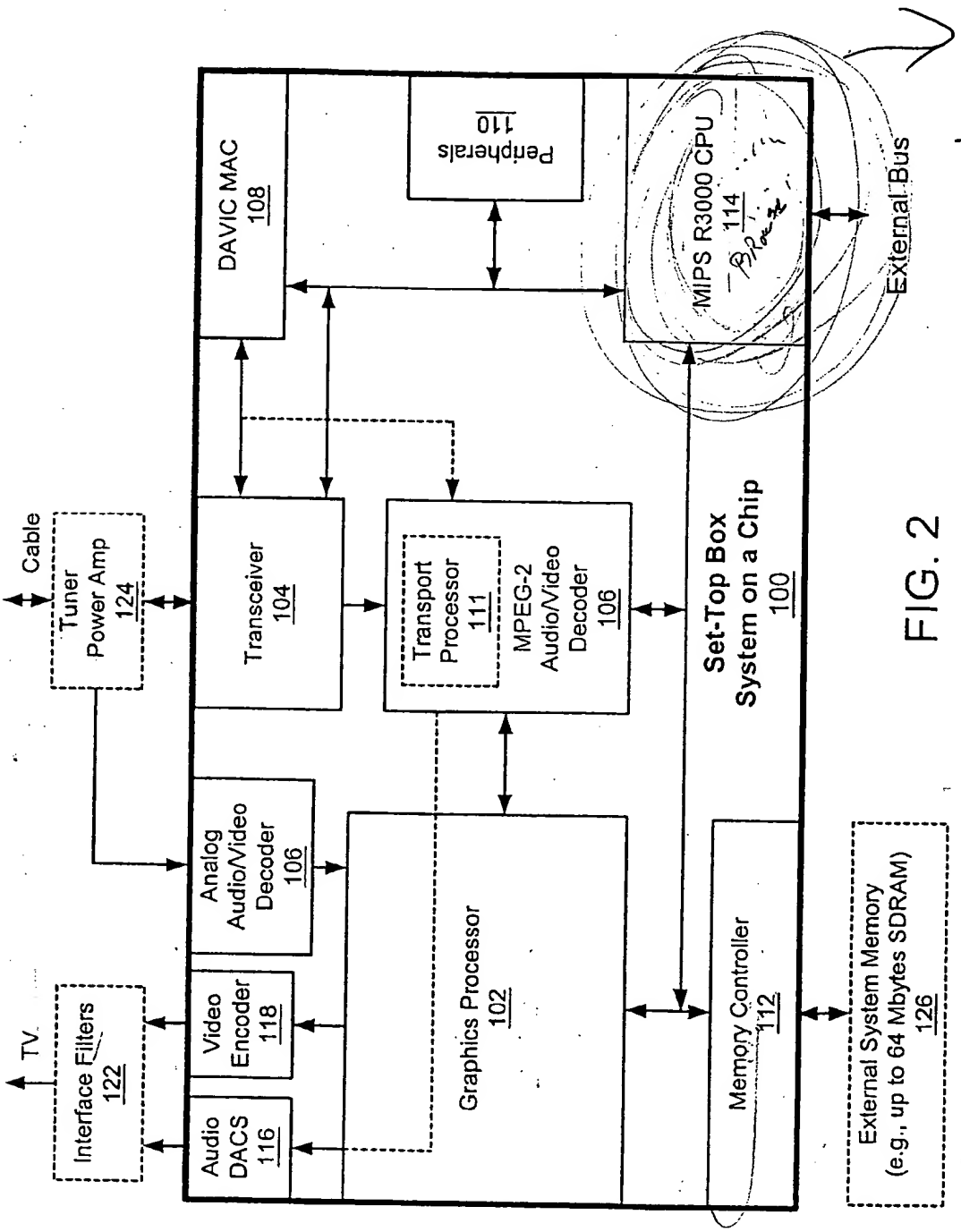
Set-Top Box System on a Chip 100
MIPS R3000 CPU 114
External Bus
DAVIC MAC 108
Peripherals 110
Transceiver 104
Transport Processor 111
MPEG-2 Audio/Video Decoder 106
Analog Audio/Video Decoder 106
Graphics Processor 102
Memory Controller 112
External System Memory (e.g., up to 64 Mbytes SDRAM) 126
Cable
Tuner Power Amp 124
TV
Interface Filters 122
Video Encoder 118
Audio DACS 116

FIG. 2

```
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         (c) 2005 FIZ TECHNIK
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         (c) 2005 The HW Wilson Co.
File 144:Pascal 1973-2005/Jul W1
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File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
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         (c) 2002 The Gale Group
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         (c)2001 ProQuest Info&Learning
File 483:Newspaper Abs Daily 1986-2005/Jul 16
         (c) 2005 ProQuest Info&Learning

Set     Items   Description
S1       4172   STB OR SET()TOP()BOX OR SETTOP()BOX
S2       8213   STT OR SET()TOP()TERMINAL OR HCT OR HOME()COMMUNICATION()T-
             ERMINAL OR (CATV OR CABLE()TELEVISION OR CABLE OR SUBSCRIBER)-
             (3N)(BOX OR CONVERTER)
S3     414579   CPU OR CENTRAL()PROCESS?()UNIT OR PROCESSOR OR MICROPROCES-
             SOR OR MICRO()PROCESSOR
S4     302902   CONTROLLER OR MEMORY()CONTROLLER??
S5      41815   (UNIFIED OR INTEGRAT? OR COMBIN? OR INCLUD? OR JOIN? OR SI-
             NGL? OR ONE OR DISTINCT??)(3N)(MEMORY OR MEMORY()MODULE)
S6       6013   AU=(LUNDBALD, J? OR LUNDBALD J? OR BALDWIN, J? OR BALDWIN -
             J? OR COFFIN, L? OR COFFIN L?)
S7       7505   UMA OR UNIFIED()MEMORY()ARCHITECTURE
S8        455   (EMBED? OR INCLUD?)(3N)BROWSER
S9       1434   (MPEG OR MOVING()PICTURE()EXPERT()GROUP)(3N)DECODER
S10      5108   S3(3N)S4
S11         9   S10(3N)S5
S12         9   S11 NOT PY>2001
S13         0   S12 AND S1
S14         0   S12 AND S2
S15         0   S12 AND S7
S16         0   S12 AND S8
S17         0   S12 AND S9
S18        49   S10 AND S5
S19        40   S18 NOT S11
S20         1   S19 AND (S7:S9)
S21        37   S19 NOT PY>2001
S22         0   S21 AND (S1 OR S2)
S23        33   RD S21 (unique items)
S24        31   S23 NOT (MAGNET OR HYDRAULIC)
S25       256   (S1 OR S2) AND S3
S26        10   S25 AND S4
```

S27	0	S26 AND S5
S28	0	S27 NOT (S11 OR S20 OR S24)
S29	0	S6 AND S1
S30	1	S6 AND S2
S31	0	S30 NOT OXYGEN
S32	0	S6 AND S10

12/3,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2005 Institution of Electrical Engineers. All rts. reserv.

7042832 INSPEC Abstract Number: B2001-10-1265F-072, C2001-10-5130-039
Title: A one chip super graphics CPU **with direct** unified memory controller **suitable for car information and control system**
Author(s): Nakatsuka, Y.; Shimomura, T.; Morita, Y.; Takami, K.; Joh, M.; Narita, M.; Yamagishi, K.; Okada, Y.; Satoh, J.
Author Affiliation: Res. Lab., Hitachi Ltd., Tokyo, Japan
Conference Title: Proceedings of the IEEE 2001 Custom Integrated Circuits Conference (Cat. No.01CH37169) p.421-3
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA 582 pp.
ISBN: 0 7803 6591 7 Material Identity Number: XX-2001-01143
U.S. Copyright Clearance Center Code: 0 7803 6591 7/2001/$10.00
Conference Title: Proceedings of the IEEE 2001 Custom Integrated Circuits Conference
Conference Sponsor: IEEE Solid State Circuits Soc.; Electron Devices Soc
Conference Date: 6-9 May 2001 Conference Location: San Diego, CA, USA
Language: English
Subfile: B C
Copyright 2001, IEE

Title: A one chip super graphics CPU **with direct** unified memory controller **suitable for car information and control system**

12/3,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2005 Institution of Electrical Engineers. All rts. reserv.

6912509 INSPEC Abstract Number: B2001-06-0170J-037
Title: Solder joint failure analysis using FEM techniques of a silicon based system-in-package
Author(s): Goetz, M.; Zahn, B.
Author Affiliation: Alpine Microsyst., Campbell, CA, USA
Conference Title: Twenty Sixth IEEE/CPMT International Electronics Manufacturing Technology Symposium (Cat. No.00CH37146) p.70-5
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA v+388 pp.
ISBN: 0 7803 6482 1 Material Identity Number: XX-2001-00329
U.S. Copyright Clearance Center Code: 0 7803 6482 1/2000/$10.00
Conference Title: Twenty Sixth IEEE/CPMT International Electronics Manufacturing Technology Symposium
Conference Sponsor: Semicond. Equipment & Mater. Int. (SEMI); Components, Packaging, & Manuf. Technol. (CPMT) Soc
Conference Date: 2-3 Oct. 2000 Conference Location: Santa Clara, CA, USA
Language: English
Subfile: B
Copyright 2001, IEE
...Abstract: package (SiP) was designed that integrates all of a desktop computer's high-performance ICs, **including CPU** , cache **memory** , **memory controller** , and Ethernet, USB and ATAPI I/O interfaces. The primary benefits provided by this integration...

12/3,K/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

03263607 INSPEC Abstract Number: B88070750, C89002194
Title: The CVAX CMCTL-a CMOS memory controller chip
Author(s): Morgan, D.K.
Author Affiliation: Digital Equipment Corp., Hudson, MA, USA
Journal: Digital Technical Journal no.7 p.139-43
Publication Date: Aug. 1988 Country of Publication: USA
CODEN: DTJOEL
Language: English
Subfile: B C

Abstract: The CMCTL-part of the CVAX family of chips-is a high-performance ECC **memory controller** for **single - processor** systems. Implemented in Digital's CMOS technology, the CMCTL is optimized to satisfy Q-bus...

12/3,K/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

00146455 INSPEC Abstract Number: C70011650
Title: Multi-computer system
Assignee(s): General Electric Co
Patent Number: GB 1170587 Issue Date: 691112
Application Date: 661116
Priority Appl. Number: US 508/68 Priority Appl. Date: 651116
Country of Publication: UK
Language: English
Subfile: C

...Abstract: be transmitted between two processors without either of them having to stop. When a central **controller** receives from a **processor** a word which **includes** a **memory** address and the identity of another processor, it causes storage of the word in a...

12/3,K/5 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05931518 E.I. No: EIP01446711858
Title: A one chip super graphics CPU **with direct** unified memory controller **suitable for car information and control system**
Author: Nakatsuka, Y.; Shimomura, T.; Morita, Y.; Takami, K.; Joh, M.; Narita, M.; Yamagishi, K.; Okada, Y.; Satoh, J.
Corporate Source: Hitachi Research Laboratory Hitachi Ltd., Hitachi-shi, Ibaraki-ken, Japan
Conference Title: IEEE 2001 Custom Integrated Circuits Conference
Conference Location: San Diego, CA, United States Conference Date: 20010506-20010509
E.I. Conference No.: 58653
Source: Proceedings of the Custom Integrated Circuits Conference 2001. p 421-423 (IEEE cat n 01CH37169)
Publication Year: 2001
CODEN: PCICER ISSN: 0886-5930
Language: English

Title: A one chip super graphics CPU **with direct** unified memory

controller **suitable for car information and control system**

12/3,K/6 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03799095 E.I. No: EIP94011196183
Title: Memory controller with an integrated graphics processor
Author: Watkins, John; Roth, Raymond; Hsieh, Michael; Radke, William; Hejna, Donald; Kim, Byung; Tom, Richard
Corporate Source: Sun Microsystems, Inc, Mountain View, CA, USA
Conference Title: Proceedings of the 1993 IEEE International Conference on Computer Design: VLSI in Computers & Processors
Conference Location: Cambridge, MA, USA Conference Date: 19931003-19931006
E.I. Conference No.: 19834
Source: Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors 1993. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA,(IEEE cat n 93CH3335-7). p 324-338
Publication Year: 1993
CODEN: PIIPE6 ISBN: 0-8186-4230-0
Language: English

Identifiers: **Memory controller** ; **Integrated** programmable graphics **processor** ; Integer vector processor; SX graphics accelerator

12/3,K/7 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03387151 E.I. Monthly No: EI9203030906
Title: PC chip set eases design of cache-based computers.
Author: Bursky, Dave
Source: Electronic Design v 38 n 19 Oct 11 1990 p 117-118
Publication Year: 1990
CODEN: ELODAW ISSN: 0013-4872
Language: English

...Abstract: be built with as few as 25 components. The only other devices needed are the **CPU** , BIOS **memory** , keyboard **controller** , an **integrated** peripheral controller (such as the widely available 82C206), and a few TTL chips.

12/3,K/8 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01232145 E.I. Monthly No: EIM8208-025653
Title: 32b VLSI SYSTEM.
Author: Beyers, Joseph W.; Dohse, Louis J.; Fucetola, Joseph P.; Kolesar, Michael L.; Lob, Clifford G.; Maitland, David S.; Malhotra, Arun K.; Seccombe, S. Dana; Wheeler, John K.; Zeller, Eugene R.
Corporate Source: Hewlett-Packard Co, Fort Collins, Colo, USA
Conference Title: Digest of Technical Papers - 1982 IEEE International Solid-State Circuits Conference.
Conference Location: San Francisco, Calif, USA Conference Date: 19820210

E.I. Conference No.: 00629
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference v 25 1982. Publ by Lewis Winner, Coral Gables, Fla, USA. Available from IEEE Serv Cent (Cat n 82CH1680-8), Piscataway, NJ, USA p 128-129
Publication Year: 1982
CODEN: DTPCDE
Language: English

Identifiers: VLSI PROCESSING SYSTEMS; FULL **INTEGRATION** ; **MEMORY** SUBSYSTEMS; **CPU** ; **MEMORY CONTROLLERS** ; **SPARE MEMOR** Y CHIPS; HAMMING DECODING; CLOCK GENERATOR CHIPS

12/3,K/9 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01535938 ORDER NO: AAD97-09569
ARCHITECTURE AND TECHNOLOGY TRADEOFFS IN THE DESIGN OF HIGH PERFORMANCE MICROPROCESSOR-BASED SYSTEMS (VLSI, CACHE HIERARCHIES, SUPERSCALAR, BUS UTILIZATION, ALPHA 21064A)
Author: ALBONESI, DAVID HENRY
Degree: PH.D.
Year: 1996
Corporate Source/Institution: UNIVERSITY OF MASSACHUSETTS (0118)
Source: VOLUME 57/10-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 6432. 176 PAGES

...design of CC-NUMA multiprocessors using the 8-way superscalar microprocessor. The results demonstrate that **integrating** the main **memory controller** onto the **microprocessor** die considerably reduces bus utilization and improves multiprocessor performance by as much as 35%. Interleaving...

20/3,K/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

05070374 JICST ACCESSION NUMBER: 02A0169787 FILE SEGMENT: JICST-E
System LSI Technologies for Mobile and Digital Consumer Products. Single-Chip Digital TV LSI.
KAI NAOYUKI (1); NAGOYA TETSUO (1); MANAKA SHIGEYUKI (1)
(1) Toshiba Corp.
Toshiba Rebyu(Toshiba Review), 2002, VOL.57,NO.1, PAGE.47-49, FIG.2, TBL.2, REF.2
JOURNAL NUMBER: F0360AAK ISSN NO: 0372-0462 CODEN: TORBA
UNIVERSAL DECIMAL CLASSIFICATION: 681.325/.326.009.16
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

...ABSTRACT: host processor as well as peripheral modules. This LSI lowers the system cost by utilizing **unified memory architecture** (**UMA**) with a 64-bit double data rate (DDR) synchronous DRAM (SDRAM) system. It integrates a configurable media **processor** as a **controller** for the dedicated hardware modules. A section filtering accelerator is implemented in the controller by...
...DESCRIPTORS: **integrated** circuit **memory** ;

24/3,K/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5464886 INSPEC Abstract Number: C9702-5310-002
Title: An advanced 3D frame buffer memory controller
Author(s): Makris, A.; White, M.; Lister, P.
Author Affiliation: Centre for VLSI & Comput. Graphics, Sussex Univ., Brighton, UK
Conference Title: Eleventh Eurographics Workshop on Graphics Hardware p.25-37
Editor(s): Schneider, B.-O.; Schilling, A.
Publisher: IBM T J Watson Res. Center, Yorktown Heights, NY, USA
Publication Date: 1996 Country of Publication: USA 144 pp.
Material Identity Number: XX96-02512
Conference Title: Proceedings of Eleventh Eurographics Workshop on Graphics Hardware
Conference Date: 26-27 Aug. 1996 Conference Location: Poitiers, France
Language: English
Subfile: C

...Abstract: of an advanced 32 bit 3D frame buffer memory controller for a 3D Graphics Raster **Processor** called TAYRA. This **memory controller** is designed to provide a performance of 33 MPixels/s for read and write cycles...

...of these memories. Also, we support up to 4 screen buffers, 16 MBytes of screen **memory** and many **combinations** of **memory** organisations up to 1600*1280.

24/3,K/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

03730506 INSPEC Abstract Number: B90060554, C90063382
Title: FPC: a floating-point processor controller **chip for systolic signal processing**
Author(s): Smith, R.; Sobelman, G.; Luk, G.; Suda, K.; Bracken, J.
Author Affiliation: Dept. of Electr. Eng. & Comput. Sci., Illinois Univ., Chicago, IL, USA
Conference Title: Proceedings. 1989 IEEE International Conference on Computer Design: VLSI in Computers and Processors (Cat. No.89CH2794-6) p.14-17
Publisher: IEEE Comput. Soc. Press, Washington, DC, USA
Publication Date: 1989 Country of Publication: USA xvii+587 pp.
ISBN: 0 8186 1971 6
U.S. Copyright Clearance Center Code: CH2794-6/89/0000-0014$01.00
Conference Sponsor: IEEE
Conference Date: 2-4 Oct. 1989 Conference Location: Cambridge, MA, USA
Language: English
Subfile: B C

Title: FPC: a floating-point processor controller **chip for systolic signal processing**
...Abstract: a 32-b instruction word that provides concurrent use of all cell resources. Additional features **include** a program **memory** , two data streams, and three control streams. The novel architectural features of the cell are...

Identifiers: floating-point **processor** **controller** chip...

24/3,K/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

03418827 INSPEC Abstract Number: C89048726
Title: A high performance VLSI computer architecture for computer graphics
Author(s): Chi-Yuan Chin; Wen-Tai Lin
Author Affiliation: General Electrical Co., Corp. Res. & Dev., Schenectady, NY, USA
Journal: Proceedings of the SPIE - The International Society for Optical Engineering vol.1001, pt.1 p.491-8
Publication Date: 1988 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
Conference Title: Visual Communications and Image Processing '88
Conference Sponsor: SPIE
Conference Date: 9-11 Nov. 1988 Conference Location: Cambridge, MA, USA
Language: English
Subfile: C

...Abstract: a global memory which are partitioned into multiple banks. Through a crossbar network, data from **one** **memory** bank can be broadcasted to many processors. Processors are physically interconnected through a hyper-crossbar...
... communication links among processors can be reconfigurated to satisfy specific dataflows of different applications. Each **processor** consists of a **controller** , arithmetic operators, local memory, a local crossbar network, and I/O ports to communicate with other processors, memory banks, and a system **controller** . Operations in each **processor** are characterized into two modes, i.e. object domain and space domain, to fully utilize...

24/3,K/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

03409000 INSPEC Abstract Number: B89050918, C89042658
Title: Picture processing for the home. The television set becomes the monitor for personal picture processing
Author(s): Miklik, W.
Journal: Elektronikschau no.3 p.28, 30-3
Publication Date: March 1989 Country of Publication: Austria
CODEN: ELTRDY ISSN: 0254-4318
Language: German
Subfile: B C

...Abstract: system designed for incorporation into digital television receivers. The system schematic diagram is shown, and **includes** picture field **memory** comprising 9 dual port DRAMs, SDA 9099 memory sync **controller** , SDA 9090 picture **processor** , SDA 9093 memory output interface, and other elements. Featurebox 88 provides better picture quality, freedom...

24/3,K/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

03399092 INSPEC Abstract Number: B89042229, C89038139
Title: The design of graphics display hardware for personal computers
Author(s): Crosshall, W.J.
Conference Title: Ausgraph 88 Proceedings p.263-70
Publisher: Australasian Comput. Graphics Assoc, Parkville, Vic., Australia
Publication Date: 1988 Country of Publication: Australia 344 pp.
Conference Date: 4-8 July 1988 Conference Location: Melbourne, Vic., Australia
Language: English
Subfile: B C

...Abstract: a 32-bit microprocessor which has been designed to serve the function of the display **controller** , display **processor** and the arbitration logic in a graphics display system) and the TMS4461 (a 64 k...
...Descriptors: **integrated memory** circuits

24/3,K/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

02947994 INSPEC Abstract Number: B87052614, C87047172
Title: MMU with integrated cache
Author(s): Lawthers, P.C.
Author Affiliation: AT&T Microelectronics, Munchen, West Germany
Journal: Elektronik Journal vol.22, no.6 p.82, 84, 86, 88, 90
Publication Date: 19 March 1987 Country of Publication: West Germany
CODEN: EKTJAY ISSN: 0013-5674
Language: German
Subfile: B C

...Abstract: cache module, WE32206 floating-point processor, WE32202 clock generator, WE32104 DMA controller and WE32103 DRAM **controller** . The **CPU** has addressing capability for 4 Gbyte memory, separate 32-bit address and data buses, 32...

... Fortran, Cobol. The interrupt structure has 15 levels. High-speed operation is enhanced by the **combined** 4 Kbyte cache **memory** and memory-management unit operating in 'write-through' mode. Hit rate is said to be...

24/3,K/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

02815792 INSPEC Abstract Number: B87011968, C87011332
Title: 82786 graphics coprocessor
Author(s): Dhacze, G.
Journal: PT/Elektrotechniek Elektronica vol.41, no.10 p.71-6
Publication Date: Oct. 1986 Country of Publication: Netherlands
CODEN: PEELDD ISSN: 0032-4086
Language: Dutch
Subfile: B C

...Abstract: by providing two processors-one for graphics (links command list in system memory to graphics **memory**) and **one** for displaying

(copies parts of bit maps onto screen). The remaining hardware includes interfaces, DRAM **controller** and **CPU** . The author discussed the software at length and explains the commands and how the display...

24/3,K/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC
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02608369 INSPEC Abstract Number: B86014253, C86013282
Title: All aboard (National Semiconductor computer boards)
Author(s): Leduc, B.
Journal: Elektronik vol.34, no.21 p.238, 240-2
Publication Date: 18 Oct. 1985 Country of Publication: West Germany
CODEN: EKRKAR ISSN: 0013-5658
Language: German
Subfile: B C

...Abstract: computers based on the NS 32000 microprocessor family. The ICM3216 modules comprise a CPU board, **one** or two **memory** boards and optional personality boards. The I/O channel **controller** includes a Z80B **microprocessor** . Software support includes Unix, C and FORTRAN.

24/3,K/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC
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02340356 INSPEC Abstract Number: B84058413, C84049720
Title: Memory controller gives a microprocessor a big mini's throughput
Author(s): Kaplinsky, C.; Freeman, M.
Author Affiliation: Signetics Corp., Sunnyvale, CA, USA
Journal: Electronic Design vol.32, no.17 p.153-64
Publication Date: 23 Aug. 1984 Country of Publication: USA
CODEN: ELODAW ISSN: 0013-4872
Language: English
Subfile: B C

Title: Memory controller gives a microprocessor a big mini's throughput
...Abstract: not live up to expectations, even when surrounded with an expensive boardful of components. A **single** smart **memory** management chip remedies this situation. It controls a hierarchy of memories-cache, main, and local...

24/3,K/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC
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01878602 INSPEC Abstract Number: B82034896, C82026842
Title: A 32b VLSI system
Author(s): Beyers, J.W.; Dohse, L.J.; Fucetola, J.P.; Kolesar, M.L.; Lob, C.G.; Maitland, D.S.; Malhotra, A.K.; Seccombe, S.D.; Wheeler, J.K.; Zeller, E.R.
Author Affiliation: Hewlett-Packard Co., Fort Collins, CO, USA
Conference Title: 1982 IEEE International Solid-State Circuits Conference Digest of Technical Papers p.128-9, 309
Publisher: IEEE, New York, NY, USA

Publication Date: 1982 Country of Publication: USA 404 pp.
Conference Sponsor: IEEE
Conference Date: 10-12 Feb. 1982 Conference Location: San Francisco, CA, USA
Language: English
Subfile: B C

Abstract: The system consists of the following VLSI chips: a 32b CPU, an I/O **processor** , a **memory controller** , a 128Kb RAM, a 640Kb ROM, and a clock generator chip, all fabricated in a...
...Descriptors: **integrated memory** circuits

24/3,K/11 (Item 11 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2005 Institution of Electrical Engineers. All rts. reserv.

01624196 INSPEC Abstract Number: B81005838
Title: Edge-mounted chip assembly for microprocessors
Author(s): Stoller, H.I.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.23, no.2 p.581-2
Publication Date: July 1980 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Subfile: B

...Abstract: the major surface of a 'master' chip. The 'master' chip may be, for example, a **microprocessor** or a **memory controller** chip. The 'slave' chips may be I/O chips or **memory** chips. Other **combinations** are also possible.

24/3,K/12 (Item 12 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2005 Institution of Electrical Engineers. All rts. reserv.

01211617 INSPEC Abstract Number: C78017535
Title: An approach to microcomputing with bit-slice microprocessor
Author(s): Smith, R.J.; Clapper, S.L.
Author Affiliation: RCA, Missile & Surface Radar, Moorestown, NJ, USA
Conference Title: Proceedings of Micro-Delcon the Delaware Bay Microcomputer Conference p.58-62
Publisher: IEEE, New York, NY, USA
Publication Date: 1978 Country of Publication: USA 68 pp.
Conference Sponsor: IEEE
Conference Date: 2 March 1978 Conference Location: Newark, DE, USA
Language: English
Subfile: C

...Abstract: These include the register arithmetic logic unit (RALU) which is also called the bit-slice **microprocessor** , the microprogram **controller** , microprogram memory and macroprogram **memory** . Software topics **include** a summary of the approach taken for software development.

24/3,K/13 (Item 13 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2005 Institution of Electrical Engineers. All rts. reserv.

01172238 INSPEC Abstract Number: B78013963, C78008847
Title: Designing the PPS 4/1
Author(s): Carlson, R.; Spence, J.
Author Affiliation: Electronic Devices Div., Rockwell Internat., El Segundo, CA, USA
Conference Title: EASCON-77 p.32-2A/5 pp.
Publisher: IEEE, New York, NY, USA
Publication Date: 1977 Country of Publication: USA xxiv+784+40 (suppl.) pp.
Conference Sponsor: IEEE
Conference Date: 26-28 Sept. 1977 Conference Location: Arlington, VA, USA
Language: English
Subfile: B C

...Abstract: one-chip calculator circuits. Classical microprocessor architecture lends itself to easy design restructuring for different **controller** and general purpose **microprocessor** applications. The powerful instruction set, universal I/O and low power drain of these circuits...
...Descriptors: **integrated memory** circuits

24/3,K/14 (Item 14 from file: 2)
DIALOG(R)File 2:INSPEC

00277312 INSPEC Abstract Number: C71015325
Title: Data processor **-peripheral transfer** controller
Assignee(s): Plessey Co. Ltd
Patent Number: GB 1225252 Issue Date: 710317
Application Date: 680307
Priority Appl. Number: GB 17361/67 Priority Appl. Date: 670414
Country of Publication: UK
Language: English
Subfile: C

Title: Data processor **-peripheral transfer** controller
Abstract: A central processor **includes** a **memory** storing data and data transfer control words, and in response to a transfer demand from...

... address at which a transfer control word is stored, are generated, the transfer control words **including** a **memory** address for data to be transferred and an instruction code for controlling the processor while...

24/3,K/15 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1634802 NTIS Accession Number: AD-A245 775/2
Video-Text Processing by Using Motorola 68020 CPU and its Environment (Master's thesis)
Hekimoglu, M. K.
Naval Postgraduate School, Monterey, CA.
Corp. Source Codes: 019895000; 251450
Mar 91 47p
Languages: English Document Type: Thesis
Journal Announcement: GRAI9210
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S.

customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A03/MF A01

... Video-Text Generation. Therefore, it is named 'VTG (Video-Text Generator)'. VTG consists of a **CPU** (MC68020), CRT **Controller** (MC6845), and DUART (MC6868). The CRT Controller processes and generates the NTSC standard video-synchronization...

... its parallel port, with peripherals. The VTG has four 32 KB of RAM for main **memory** and **one** 16 KB of RAM for the CRT Controller Refresh Memory. The system software and the...

24/3,K/16 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05448066 E.I. No: EIP99124954713
Title: Storage hierarchy to support a 600 MHz G5 S/390 microprocessor
Author: Turgeon, Paul R.; Mak, Pak-kin; Plass, Donald; Blake, Michael; Fee, Michael; Fischer, Mark; Ford, Carl; Holmes, Glenn; Jackson, Kathy; Jones, Christine; Kark, Kevin; Malgioglio, Frank; Meaney, Patrick; Pell, Edwin; Scarpero, William; et al
Corporate Source: IBM Corp, Poughkeepsie, NY, USA
Conference Title: Proceedings of the 1999 46th IEEE International Solid-State Circuits Conference (ISSCC'99)
Conference Location: San Francisco, CA, USA Conference Date: 19990215-19990217
E.I. Conference No.: 55474
Source: Digest of Technical Papers - IEEE International Solid-State Circuits Conference 1999. p 90-91
Publication Year: 1999
CODEN: DTPCDE ISSN: 0193-6530
Language: English

...Abstract: G4. In particular, performance improvement has been achieved with an L2 cache, system controller and **memory** interface clocked at **one** half the microprocessor frequency. 5 Refs.
Identifiers: Storage hierarchy; System **controller** ; **Microprocessor** frequency; Static random access memory; Symmetric multiprocessor

24/3,K/17 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04850706 E.I. No: EIP97103881138
Title: World's first single-chip solution for 100 Hz core
Author: Benning, Herwig A.
Corporate Source: Semiconductor Group
Source: Components v 32 n 4 1997. p 20-22
Publication Year: 1997
CODEN: 002455 ISSN: 9173-1734
Language: English

...Abstract: the world's first 100 Hz IC, the SDA 9255 is equipped with on-chip **integrated memory** . This allows 100 Hz technology to be integrated into television sets at very low cost...

...addition to the core components, Siemens also supplies the 100 Hz front end, the display **processor** and digital deflection **controller** specially developed for 100 Hz. This means that all the ICs required for a 100...

24/3,K/18 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04276152 E.I. No: EIP95102907500
Title: Programming TI's multimedia video processor
Author: May, William
Source: Dr. Dobb's Journal of Software Tools for Professional Programmer v 20 n 11 Nov 1995. 5pp
Publication Year: 1995
CODEN: DDJTEQ ISSN: 1044-789X
Language: English

...Abstract: capable of accurately performing two billion operations per second, it also has several limitations which **include** cycles, **memory** , and bandwidth.
Identifiers: Multimedia video processor; Client/server programs; Real-time video; Master **processor** ; Multitasking kernel; Transfer **controller**

24/3,K/19 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04162758 E.I. No: EIP95052711689
Title: PA 7100LC microprocessor: a case study of IC design decisions in a competitive environment
Author: Bass, Mick; Knebel, Patrick; Quint, David W.; Walker, William L.
Source: Hewlett-Packard Journal v 46 n 2 Apr 1995. p 12-22
Publication Year: 1995
CODEN: HPJOAX ISSN: 0018-1153
Language: English

...Abstract: to the creation of a low-cost, single-chip processor core - the PA 7100LC - that **includes** a built-in **memory** controller, a **combined** variable-size off-chip primary instruction and data cache, a 1K-byte on-chip instruction...
Identifiers: PA 7100LC microprocessor; **Central processing unit** ; Design decision; **Memory controller** ; I/O controller; Floating point unit

24/3,K/20 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02945757 E.I. Monthly No: EIM9008-034493
Title: Fault tolerant power controller.
Author: Gudea, Denny D.; Barany, Frank
Corporate Source: TRW, Redondo Beach, CA, USA
Conference Title: Proceedings of the 24th Intersociety Energy Conversion Engineering Conference - IECEC-89. Part 1 (of 6): Aerospace Power Systems and Power Conditioning
Conference Location: Washington, DC, USA Conference Date: 19890806

E.I. Conference No.: 13351
Source: Proceedings of the Intersociety Energy Conversion Engineering Conference v 1. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA. Available from IEEE Service Cent (cat n 89CH2781-3), Piscataway, NJ, USA. p 231-237
Publication Year: 1989
CODEN: PIECDE ISSN: 0146-955X
Language: English

...Abstract: and associated hardware and software are presented. The fault tolerance is achieved at multiple levels. **Single** -bit **memory** errors are corrected by Hamming codes. Larger memory errors are corrected by requesting database information...
Identifiers: REDUNDANT CONTROLLER; POWER **CONTROLLER** ; RADIATION-HARDENED **MICROPROCESSOR** ; HAMMING CODES; LANDSAT POWER SWITCHING UNIT; **SINGLE** -BIT **MEMORY** ERRORS

24/3,K/21 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02633241 E.I. Monthly No: EI8809080748
Title: MEMORY ATE. ATE CONSIDERATIONS FOR BOARD AND SYSTEM TEST.
Author: Anon
Corporate Source: Micro Control Co,, Minneapolis, MN, USA
Source: Evaluation Engineering v 27 n 4 Apr 1988 p 14, 16, 18-19
Publication Year: 1988
CODEN: EVENAE ISSN: 0014-3316
Language: English

...Abstract: the system. Three available types of board test systems are considered: in-circuit, functional and **combinational** . A **memory** and logic test system block diagram is shown which incorporates the features necessary to provide...

...functional testing of boards and systems. The test system consists of these components: a programmable **controller** , a pattern **processor** , a timing system, power supplies, and interface, software and associated options.

24/3,K/22 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02551079 E.I. Monthly No: EIM8803-013344
Title: VL86C010 RISC FAMILY.
Author: Stockton, John F.; Farrell, James J.
Corporate Source: VLSI Technology Inc, Phoenix, AZ, USA
Conference Title: Electro/87 and Mini/Micro Northeast Conference Record.
Conference Location: New York, NY, USA Conference Date: 19870407
E.I. Conference No.: 10729
Source: Conference Record - Electro 1987. Publ by Electronic Conventions Management, Los Angeles, CA, USA p 10. 2. 1-10. 2. 9
Publication Year: 1987
CODEN: ELCRDH
Language: English

...Abstract: paper presents an overview of the VL86C010 RISC processor

and its family of peripheral components **including** a **Memory** Controller, Video Controller and an I/O controller. Detailed information is presented of the processor...
Identifiers: RISC **PROCESSOR** ; VIDEO **CONTROLLER** ; I/O CONTROL

24/3,K/23 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online
(c) 2005 ProQuest Info&Learning. All rts. reserv.

1068268 ORDER NO: AAD89-14365
GOB: A GRAPHICAL OBJECT BASED DISPLAY ARCHITECTURE
Author: KELLY, JOHN CAREY, JR.
Degree: PH.D.
Year: 1988
Corporate Source/Institution: UNIVERSITY OF DELAWARE (0060)
Source: VOLUME 50/04-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 1569. 286 PAGES

...DMA transfer and a 12.5 million bits per second fiber optic link. A fast **processor** in the display **controller** interprets the image descriptor and produces commands to the image creation/display hardware. Images are created by **combining** objects from a **memory** containing objects into a bit-map output buffer. This update occurs fast enough to support...

24/3,K/24 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
(c)2005 Japan Science and Tech Corp(JST). All rts. reserv.

02582110 JICST ACCESSION NUMBER: 95A0629075 FILE SEGMENT: JICST-E
Cached DRAM Application in Personal Computer. High Performance of Personal Computer by Cached DRAM.
TOMIOKA TAKANORI (1); OTA MAKOTO (1); OGAWA TOSHIYUKI (2); TOYOMOTO HIDEHARU (2)
(1) Mitsubishidenkisemikondakutasofutoea; (2) Mitsubishi Electr. Corp., Kita-Itami Work.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1995, VOL.95,NO.117(ED95 46-57), PAGE.23-30, FIG.8, TBL.2, REF.3
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 681.325/.327
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

...ABSTRACT: fundamental advantage over a conventional DRAM/SRAM cache. We made a system with sixteen 4MCDRAMs, **controller** and **CPU** to connect PC motherboard. The system has only 32KB cache memory but its performance is...
...DESCRIPTORS: **integrated** circuit **memory** ;

24/3,K/25 (Item 1 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management
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01252869 E98100329258

Stromspar-Tricks bei Embedded Controllern
Rally, MS
Design und Elektronik Themenheft, v46, n10 DSPs und Mikrocontroller, pp104-108, 1998
Document type: journal article Language: German
Record type: Abstract
ISSN: 0933-8667

ABSTRACT:
...mW) bei einer 25 MHz betriebenen CPU im Dhrystone-Benchmark-Test auf die verschiedenen Funktionen **CPU** (69 %), DRAM- **Controller** (18 %) und uebrige Peripherie (13 %); die Abschaltbarkeit des Taktes einzelner Peripheriefunktionen; die drei grundlegenden Leistungsspar...

...chipinternen Peripherie anhand eines Kurvendiagramms mit der Leistungsaufnahme als Funktion der Kapazitaet der SIMM-Adressanschluesse (**Single** Inline **Memory Module**) und einer Messwerttabelle ueber die Leistungsaufnahme des Bausteins in drei verschiedenen DMA-Betriebsarten (Direct Memory...
...IDENTIFIERS: **SINGLE** INLINE **MEMORY MODULE**); Stromeinsparung; Verlustleistung; Embedded-Controller

24/3,K/26 (Item 2 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00773822 I94055230286
A low-cost graphics and multimedia workstation chip set
(Ein kostenguenstiger Chip-Set fuer graphische und Multimedia-Workstations)
Undy, S; Bass, M; Hollenbeck, D; Kever, W; Thayer, L
Hewlett-Packard Co., Fort Collins, CO, USA
IEEE Micro, v14, n2, pp10-22, 1994
Document type: journal article Language: English
Record type: Abstract
ISSN: 0272-1732

ABSTRACT:
...floating-point unit, a 1-Kbyte internal instruction cache, an integrated external cache controller, an **integrated memory** and I/O controller, plus enhancements for little-endian and multimedia applications. Its Artist graphics...
IDENTIFIERS: COMPUTER GRAPHIC EQUIPMENT; HEWLETT PACKARD COMPUTERS; MULTIMEDIA WORKSTATION CHIP SET; HUMMINGBIRD **MICROPROCESSOR** ; ARTIST GRAPHICS **CONTROLLER** ; GRAPHICAL USER INTERFACE; VIDEO CONTROLLER; GRAPHICS WORKSTATION; CHIP SET; GRAPHISCHE WORKSTATION; Multimedia; Workstation; Graphikprozessor; Chipset

24/3,K/27 (Item 3 from file: 95)
DIALOG(R)File 95:TEME-Technology & Management

00561850 I92025599937
Reliability analysis of a computer system for a data collection application
(Analyse der Zuverlaessigkeit eines Kleinrechnersystems fuer Datenerfassung)
Reibman, A
AT&T Bell Lab., Holmdel, NJ, USA
Proceedings. 1990 IEEE International Conference on Computer Design: VLSI in

Computers and Processors, 17-19 Sept. 1990, Cambridge, MA, USA1990
Document type: Conference paper Language: English
Record type: Abstract
ISBN: 0-8186-2079-X

ABSTRACT:
...platform that serves as a database manager and transaction processor. The components of the platform **include** the processor, **memory** , I/O cards, power supply, and the disks and disk controller. Users have workstations that...
...IDENTIFIERS: POWER SUPPLY; LOCAL AREA NETWORK; DISK MIRRORING; TEST POINTS; CENTRAL MINICOMPUTER PLATFORM; DATABASE MANAGER; TRANSACTION **PROCESSOR** ; DISK **CONTROLLER** ; CENTRAL **PROCESSOR** ; DATA COLLECTION POINTS; WIDE AREA NETWORK; DISK SUBSYSTEMS; RELIABILITY BOTTLENECK; RELIABILITY IMPROVEMENT; SPEICHER; Rechnernetz; Datenerfassung...

24/3,K/28 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1143839 H.W. WILSON RECORD NUMBER: BAST94012392
Intel/VLSI join the PDA fray
Statt, Paul;
Byte v. 19 (Jan. '94) p. 101-5
DOCUMENT TYPE: Feature Article ISSN: 0360-5280

...ABSTRACT: chip set for personal digital assistants. The core of this chip set is the Integrated **Processor Controller** , featuring a fully static Intel 32-bit CPU (based on the Intel 386) that includes...

...logic for the architecture, which is housed in a 176-pin thin quad flat package, **integrates** such functions as **memory** management, video control, and power management. The architecture of the chip set and the outlook...

24/3,K/29 (Item 2 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

1090783 H.W. WILSON RECORD NUMBER: BAST93022868
Local memory coaxes top speed from SCSI masters
Paulsen, Erik;
Electronic Design v. 41 (Apr. 15 '93) p. 75-6+
DOCUMENT TYPE: Feature Article ISSN: 0013-4872

ABSTRACT: Faster data transfer can be achieved by using SCSI bus mastering **combined** with local dedicated **memory** . SCSI host adapters can be divided into 3 types: CPU assisted, DMA slave, and bus master. The bus master SCSI adapter is the fastest because it possesses its own embedded **processor** and DMA **controller** , thereby allowing it to bypass the DMA **controller** and main **processor** . Placing the SCSI bus master controller on its own dedicated bus with local dedicated memory...

24/3,K/30 (Item 1 from file: 583)
DIALOG(R)File 583:Gale Group Globalbase(TM)

05302396

The Olympus Image Systems Inc
  US - OLYMPUS IMAGE SYSTEMS LAUNCHES IMAGING PRINTER
Computergram International (CGI) 7 September 1992 p1
ISSN: 0268-716X

... the print cartridge and operator maintenance kit require changing every 100k pages. The Olympus IS2030 **controller processor** has 4Mb memory expandable to 28Mb, and it accepts **Single** In-Line **Memory** Modules. The controller has a Microsoft Corp TrueImage PostScript interpreter and Hewlett-Packard Co LaserJet...

24/3,K/31 (Item 2 from file: 583)
DIALOG(R)File 583:Gale Group Globalbase(TM)

03752254
AMD UNVEILS ONE-CHIP 80286 PROCESSOR BOARD
  US - AMD UNVEILS ONE-CHIP 80286 PROCESSOR BOARD
Computergram International (CGI) 2 October 1990 p1
ISSN: 0268-716X

... microprocessor with all the support circuitry necessary to build an AT-alike apart from the **memory** chips **integrated** with the CPU on a single chip. Aimed particularly at the portable computer market, the...

... versions of its microprocessors. Intel's own highly integrated 80386SX will include 80387SX maths co-**processor** , cache **memory controller** , small cache and peripheral logic, and possibly a VGA-compatible graphics circuit with the CPU...

```
File 344:Chinese Patents Abs Aug 1985-2005/May
         (c) 2005 European Patent Office
File 347:JAPIO Nov 1976-2005/Feb(Updated 050606)
         (c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200545
         (c) 2005  Thomson Derwent

Set     Items   Description
S1       5942   STB OR SET()TOP()BOX OR SETTOP()BOX
S2       5229   STT OR SET()TOP()TERMINAL OR HCT OR HOME()COMMUNICATION()T-
             ERMINAL OR (CATV OR CABLE()TELEVISION OR CABLE OR SUBSCRIBER)-
             (3N)(BOX OR CONVERTER)
S3     620929   CPU OR CENTRAL()PROCESS?()UNIT OR PROCESSOR OR MICROPROCES-
             SOR OR MICRO()PROCESSOR
S4     760637   CONTROLLER OR MEMORY()CONTROLLER??
S5      76898   (UNIFIED OR INTEGRAT? OR COMBIN? OR INCLUD? OR JOIN? OR SI-
             NGL? OR ONE OR DISTINCT??)(3N)(MEMORY OR MEMORY()MODULE)
S6        437   AU=(LUNDBALD, J? OR LUNDBALD J? OR BALDWIN, J? OR BALDWIN -
             J? OR COFFIN, L? OR COFFIN L?)
S7         68   UMA OR UNIFIED()MEMORY()ARCHITECTURE
S8        542   (EMBED? OR INCLUD?)(3N)BROWSER
S9       1471   (MPEG OR MOVING()PICTURE()EXPERT()GROUP)(3N)DECODER
S10      1472   (S1 OR S2) AND S3
S11       203   S10 AND S4
S12        11   S11 AND S5
S13         1   S12 AND S7
S14         0   S12 AND S8
S15         1   S12 AND S9
S16         0   S15 NOT S13
S17        10   S12 NOT (S13 OR S15)
S18         1   S17 NOT PY>2001
S19         3   S17 AND AD=20000501:20010509/PR
S20         2   S19 NOT S18
S21         0   S6 AND S11
S22        41   S6 AND IC=H04N?
S23        41   IDPAT (sorted in duplicate/non-duplicate order)
S24        38   IDPAT (primary/non-duplicate records only)
S25         9   S24 AND (S1 OR S2)
S26         2   S25 AND S3
S27         0   (S25 OR S26) AND S4
S28         1   (S25 OR S26) AND S5
S29         6   S25 NOT (S26 OR S28)
S30         0   S29 NOT PY>2001
```

13/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015367704 **Image available**
WPI Acc No: 2003-428642/200340
XRPX Acc No: N03-342153
Interactive set - top box **for television system, has graphics** processor **and** central processing unit **connected to memory and** memory controller **of memory has buffers and arbiters**
Patent Assignee: TERALOGIC INC (TERA-N)
Inventor: AULD D R; HOLMER B K; HUANG H J; YEH G K
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6526583	B1	20030225	US 99263454	A	19990305	200340	B

Priority Applications (No Type Date): US 99263454 A 19990305
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6526583	B1		29	H04N-007/173	

Interactive set - top box **for television system, has graphics** processor **and** central processing unit **connected to memory and** memory controller **of memory has buffers and arbiters**

Abstract (Basic):
... The **set - top box** has a graphics **processor** (350) and **central processing unit** (340) connected to memory (325). The **memory** has a **controller including** client interface arbiter connected to client buffer, client priority arbiter, bank buffer, bank priority arbiter. The decoders (315,310) receiving analog and digital signals respectively are connected to the graphics **processor** .
... 1) **memory controller** ;
(...

...3) graphics **processor** ; and...

...4) video display **controller** .
...

...Interactive **set - top box** with **unified memory architecture** e.g. Internet TV box, smart television, Internet television, digital video disk system for interactive...

...The figure shows the block diagram of **set - top box** .
...
... **central processing unit** (340...

...graphics **processor** (350
Technology Focus:
... The decoder connected to the graphics **processor** confirms to any one of the standard MPEG-1, MPEG-2 or MPEG-4. The...
...Title Terms: **PROCESSOR** ;
?

18/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014285068 **Image available**
WPI Acc No: 2002-105769/200214
Related WPI Acc No: 1999-023718; 2000-013078; 2000-070992; 2000-104934; 2000-586963; 2000-663635; 2001-167580; 2001-289597; 2001-315245; 2001-365929; 2002-179215; 2002-238118; 2002-442397; 2002-626910; 2002-642711; 2005-028433; 2005-329532
XRPX Acc No: N02-078700

Dynamic random access memory module used in computer system, compares uncompressed data containing multiple symbols with entries in history table in parallel fashion

Patent Assignee: ALVAREZ M J (ALVA-I); DYE T A (DYET-I); GEIGER P (GEIG-I)
Inventor: ALVAREZ M J; DYE T A; GEIGER P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20010054131	A1	20011220	US 99239659	A	19990129	200214 B
			US 99421968	A	19991020	
			US 2000491343	A	20000126	
			US 2001818283	A	20010327	

Priority Applications (No Type Date): US 2001818283 A 20010327; US 99239659 A 19990129; US 99421968 A 19991020; US 2000491343 A 20000126
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20010054131	A1		122	G06F-012/00	CIP of application US 99239659
					CIP of application US 99421968
					CIP of application US 2000491343
					CIP of patent US 6208273

Abstract (Basic):
... b) **Processor** ;
(...

...c) Cache **controller** ;
(...

...w) **Set - top box** ;
(...

...X technology is also applicable for data compression in dual-in-line memory module (DIMM), **processor** (claimed), cache **controller** (claimed), Bus bridge (claimed), solid state storage device (claimed), intelligent device (claimed), network hub (claimed...
...services digital network (ISDN) adapter (claimed), asynchronous transfer mode (ATM) adapter (claimed), network appliance (claimed), **set - top box** (claimed), digital-to-analog converter (DAC) (claimed), digital data reading system (claimed), digital data recording...

...The figure shows the block diagram illustrating the compression/decompression logic in **integrated memory controller** .

20/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

017005216 **Image available**
WPI Acc No: 2005-329532/200534
Related WPI Acc No: 1999-023718; 2000-013078; 2000-070992; 2000-104934; 2000-586963; 2000-663635; 2001-167580; 2001-289597; 2001-315245; 2001-365929; 2002-105769; 2002-179215; 2002-238118; 2002-442397; 2002-626910; 2002-642711; 2005-028433
XRPX Acc No: N05-269307

Memory management method in computer system, involves generating selects pointing to symbols in combined history window, in response to examined tokens and generating uncompressed data with symbols using selects

Patent Assignee: QUICKSHIFT INC (QUIC-N)
Inventor: ALVAREZ M J; DYE T A; GEIGER P
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6879266	B1	20050412	US 97916464	A	19970808	200534	B
			US 99239659	A	19990129		
			US 99144125	P	19990716		
			US 2000616480	A	20000714		

Priority Applications (No Type Date): US 99144125 P 19990716; US 97916464 A 19970808; US 99239659 A 19990129; US 2000616480 A 20000714
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6879266	B1		104	H03M-007/30	CIP of application US 97916464 CIP of application US 99239659 Provisional application US 99144125 CIP of patent US 6173381

Abstract (Basic):
... an embedded data compression and decompression engine, used in computer system (claimed) and digital TV **set - top box** .
...

...The figure shows a block diagram of the **integrated memory controller** (IMC...

... **memory controller** (220...

...local **CPU** interface (202

20/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014971213 **Image available**
WPI Acc No: 2003-031727/200303
XRPX Acc No: N03-025086

Multimedia processor **system has multimedia and system controllers that access main memory through** memory controller **that accepts external and internal requests**

Patent Assignee: MATSUSHITA ELECTRIC IND CO LTD (MATU); MATSUSHITA DENKI SANGYO KK (MATU)
Inventor: BI M M; CHOW K M; TANAKA T
Number of Countries: 028 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 1231543	A2	20020814	EP 20023368	A	20020213	200303 B
US 20020120709	A1	20020829	US 200268948	A	20020211	200303
JP 2002236607	A	20020823	JP 200135244	A	20010213	200303

Priority Applications (No Type Date): JP 200135244 A 20010213

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1231543	A2	E	20	G06F-015/167	
	Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR				
US 20020120709	A1			G06F-015/167	
JP 2002236607	A		14	G06F-012/00	

Multimedia processor **system has multimedia and system controllers that access main memory through** memory controller **that accepts external and internal requests**

Abstract (Basic):

... A **memory controller** accepts an external memory request from the external processors and internal request issued from the multimedia **processor** , for controlling process for arbitrated requests. A multimedia and system controllers access main **memory** through **memory controller** . **One** of the external **processor** shares **one** unit of main **memory** .

... 1) Shared **memory controller** ;

(...

...2) Multimedia **memory controller** ; and...

...Multimedia **processor** system for DVD player, DVD recorder **set top box** , etc...

...Enables external processors to access bulk memory storage device of the multimedia **processor** . Shares **single memory** for several external processors with increased performance...

...The figure shows the block diagram of the multimedia **processor** system

Title Terms: **PROCESSOR** ;

28/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015114264 **Image available**
WPI Acc No: 2003-174784/200317
XRPX Acc No: N03-137671
Set top box **for receiving and processing digital data, has** unified memory **which satisfies** memory **requirement of tuning and processing components and audio/video/data unit**
Patent Assignee: BALDWIN J A (BALD-I); COFFIN L F (COFF-I); LUNDBALD J A (LUND-I)
Inventor: **BALDWIN J A ; COFFIN L F ; LUNDBALD J A**
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020170072	A1	20021114	US 2001851841	A	20010509	200317	B

Priority Applications (No Type Date): US 2001851841 A 20010509
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020170072	A1		11	H04N-007/173	

Set top box **for receiving and processing digital data, has** unified memory **which satisfies** memory **requirement of tuning and processing components and audio/video/data unit**
Inventor: **BALDWIN J A** ...

... **COFFIN L F** ...

... **LUNDBALD J A**

Abstract (Basic):
... browser, provides control functionality for the tuning component and the A/V/D unit. A **unified memory** controlled by the processing component, satisfies memory requirements of the tuning and processing components and...
... **Set top box** such as satellite receiver and **cable box** used for receiving and processing digital data, in home entertainment system...

...the need for separate memories and reduces the cost of the system, by providing an **unified memory** which is efficiently used by the various components, when processing digital data. Enables simultaneous processing
International Patent Class (Main): **H04N-007/173**
International Patent Class (Additional): **H04N-007/16**

File 9:Business & Industry(R) Jul/1994-2005/Jul 18
(c) 2005 The Gale Group
File 15:ABI/Inform(R) 1971-2005/Jul 18
(c) 2005 ProQuest Info&Learning
File 16:Gale Group PROMT(R) 1990-2005/Jul 18
(c) 2005 The Gale Group
File 20:Dialog Global Reporter 1997-2005/Jul 19
(c) 2005 The Dialog Corp.
File 47:Gale Group Magazine DB(TM) 1959-2005/Jul 19
(c) 2005 The Gale group
File 75:TGG Management Contents(R) 86-2005/Jul W2
(c) 2005 The Gale Group
File 80:TGG Aerospace/Def.Mkts(R) 1982-2005/Jul 18
(c) 2005 The Gale Group
File 88:Gale Group Business A.R.T.S. 1976-2005/Jul 18
(c) 2005 The Gale Group
File 98:General Sci Abs/Full-Text 1984-2004/Dec
(c) 2005 The HW Wilson Co.
File 112:UBM Industry News 1998-2004/Jan 27
(c) 2004 United Business Media
File 141:Readers Guide 1983-2004/Dec
(c) 2005 The HW Wilson Co
File 148:Gale Group Trade & Industry DB 1976-2005/Jul 19
(c)2005 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
(c) 1999 The Gale Group
File 275:Gale Group Computer DB(TM) 1983-2005/Jul 19
(c) 2005 The Gale Group
File 264:DIALOG Defense Newsletters 1989-2005/Jul 18
(c) 2005 The Dialog Corp.
File 484:Periodical Abs Plustext 1986-2005/Jul W2
(c) 2005 ProQuest
File 553:Wilson Bus. Abs. FullText 1982-2004/Dec
(c) 2005 The HW Wilson Co
File 570:Gale Group MARS(R) 1984-2005/Jul 18
(c) 2005 The Gale Group
File 608:KR/T Bus.News. 1992-2005/Jul 19
(c)2005 Knight Ridder/Tribune Bus News
File 620:EIU:Viewswire 2005/Jul 18
(c) 2005 Economist Intelligence Unit
File 613:PR Newswire 1999-2005/Jul 19
(c) 2005 PR Newswire Association Inc
File 621:Gale Group New Prod.Annou.(R) 1985-2005/Jul 19
(c) 2005 The Gale Group
File 623:Business Week 1985-2005/Jul 14
(c) 2005 The McGraw-Hill Companies Inc
File 624:McGraw-Hill Publications 1985-2005/Jul 18
(c) 2005 McGraw-Hill Co. Inc
File 634:San Jose Mercury Jun 1985-2005/Jul 18
(c) 2005 San Jose Mercury News
File 635:Business Dateline(R) 1985-2005/Jul 16
(c) 2005 ProQuest Info&Learning
File 636:Gale Group Newsletter DB(TM) 1987-2005/Jul 18
(c) 2005 The Gale Group
File 647:CMP Computer Fulltext 1988-2005/Jul W1
(c) 2005 CMP Media, LLC
File 696:DIALOG Telecom. Newsletters 1995-2005/Jun 20
(c) 2005 The Dialog Corp.
File 674:Computer News Fulltext 1989-2005/Jul W3
(c) 2005 IDG Communications
File 810:Business Wire 1986-1999/Feb 28

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         (c) 1999 Business Wire
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 587:Jane`s Defense&Aerospace 2005/Jul W3
         (c) 2005 Jane`s Information Group

Set     Items   Description
S1     120235   STB OR SET()TOP()BOX OR SETTOP()BOX
S2      40558   STT OR SET()TOP()TERMINAL OR HCT OR HOME()COMMUNICATION()T-
             ERMINAL OR (CATV OR CABLE()TELEVISION OR CABLE OR SUBSCRIBER)-
             (3N)(BOX OR CONVERTER)
S3    1426682   CPU OR CENTRAL()PROCESS?()UNIT OR PROCESSOR OR MICROPROCES-
             SOR OR MICRO()PROCESSOR
S4     714383   CONTROLLER OR MEMORY()CONTROLLER??
S5     170362   (UNIFIED OR INTEGRAT? OR COMBIN? OR INCLUD? OR JOIN? OR SI-
             NGL? OR ONE OR DISTINCT??)(3N)(MEMORY OR MEMORY()MODULE)
S6       2187   AU=(LUNDBALD, J? OR LUNDBALD J? OR BALDWIN, J? OR BALDWIN -
             J? OR COFFIN, L? OR COFFIN L?)
S7      28330   UMA OR UNIFIED()MEMORY()ARCHITECTURE
S8      30715   (EMBED? OR INCLUD?)(3N)BROWSER
S9      11886   (MPEG OR MOVING()PICTURE()EXPERT()GROUP)(3N)DECODER
S10      2891   (S1 OR S2)(10N)S3
S11        87   S10(10N)S4
S12         3   S11(10N)S5
S13         1   S11(10N)S7
S14         0   S11(10N)S8
S15        12   S11(10N)S9
S16        12   S15 NOT PY>2001
S17         5   RD (unique items)
S18     38282   S3(10N)S4
S19      1680   S18(10N)S5
S20         6   S19(10N)S1
S21         5   RD (unique items)
S22         5   S21 NOT PY>2001
S23         0   S19(10N)S2
S24         0   S6(10N)S19
S25         0   S6(10N)S1
S26         0   S6(10N)S7
```

12/3,K/1 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

07926399 Supplier Number: 65353124 (USE FORMAT 7 FOR FULLTEXT)
Controller IC Is Gateway To Multiple, Secure A/V. (Technology Information)
Grossman, Steve
Electronic Design, v48, n18, p86
Sept 5, 2000
Language: English Record Type: Fulltext Abstract
Document Type: Magazine/Journal; Trade
Word Count: 2628

... systems.
A Plethora Of Buses
The STB/PVR controller IC has been configured with a **unified memory** architecture (UMA). This enables both the external **CPU** and the **STB** /PVR **controller** IC to share identical memory via the 32-bit SDRAM interface. The memory controller, which...

12/3,K/2 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

08675552 SUPPLIER NUMBER: 18293683 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Mitsubishi, NEC explore memory-MPU pairings. (Mitsubishi Electric's M32R/D microprocessor) (Product Announcement)
MacLellan, Andrew
Electronic News (1991), v42, n2116, p50(1)
May 13, 1996
DOCUMENT TYPE: Product Announcement ISSN: 1061-6624 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 775 LINE COUNT: 00064

...ABSTRACT: interested in exploring the possibility of reducing bus bandwidth tie-ups affecting multimedia applications by **integrating memory** on-chip with microprocessor functions. Mitsubishi unveiled its M32R/D **microprocessor** , designed for network **controller** , **set - top box** and personal digital assistant among other applications. The **processor combines memory** and CPU, along with peripherals in the form of an ASIC, to deliver major improvements...

12/3,K/3 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01937885 SUPPLIER NUMBER: 18293683 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Mitsubishi, NEC explore memory-MPU pairings. (Mitsubishi Electric's M32R/D microprocessor) (Product Announcement)
MacLellan, Andrew
Electronic News (1991), v42, n2116, p50(1)
May 13, 1996
DOCUMENT TYPE: Product Announcement ISSN: 1061-6624 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 775 LINE COUNT: 00064

...ABSTRACT: interested in exploring the possibility of reducing bus bandwidth tie-ups affecting multimedia applications by **integrating**

memory on-chip with microprocessor functions. Mitsubishi unveiled its M32R/D **microprocessor** , designed for network **controller** , **set - top box** and personal digital assistant among other applications. The **processor combines memory** and CPU, along with peripherals in the form of an ASIC, to deliver major improvements...

13/3,K/1 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

07926399 Supplier Number: 65353124 (USE FORMAT 7 FOR FULLTEXT)
Controller IC Is Gateway To Multiple, Secure A/V. (Technology Information)
Grossman, Steve
Electronic Design, v48, n18, p86
Sept 5, 2000
Language: English Record Type: Fulltext Abstract
Document Type: Magazine/Journal; Trade
Word Count: 2628

... systems.

A Plethora Of Buses

The STB/PVR controller IC has been configured with a **unified memory architecture** (**UMA**). This enables both the external **CPU** and the **STB** /PVR **controller** IC to share identical memory via the 32-bit SDRAM interface. The memory controller, which...

17/3,K/1 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

06279985 Supplier Number: 54414925 (USE FORMAT 7 FOR FULLTEXT)
Audio Notes.
Audio Week, v11, n16, pNA
April 19, 1999
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 1758

... will enable programmers to offer new interactive, telephony and Internet services inexpensively through TV set. **STB controller** chip, announced April 13, combines PowerPC 401 **processor** , **MPEG** video **decoder** , onboard cache and memory, as well as numerous interfaces for smart card, parallel and serial...

17/3,K/2 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

06279835 Supplier Number: 54414722 (USE FORMAT 7 FOR FULLTEXT)
DTV PROGRESSES AT NAB SHOW.
Consumer Electronics, v39, n16, pNA
April 19, 1999
Language: English Record Type: Fulltext
Document Type: Newsletter; Trade
Word Count: 684

... will enable programmers to offer new interactive, telephony and Internet services inexpensively through TV set. **STB controller** chip combines PowerPC 401 **processor** , **MPEG** video **decoder** , onboard cache and memory, as well as numerous interfaces for smart card, parallel and serial ...

17/3,K/3 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

06271855 Supplier Number: 54387132 (USE FORMAT 7 FOR FULLTEXT)
MASS MEDIA. (Brief Article)
Communications Daily, v19, n71, pNA
April 14, 1999
Language: English Record Type: Fulltext
Article Type: Brief Article
Document Type: Newsletter; Trade
Word Count: 1430

... will enable programmers to offer new interactive, telephony and Internet services inexpensively through TV set. **STB controller** chip, announced Tues., combines PowerPC 401 **processor** , **MPEG** video **decoder** , onboard cache and memory, as well as numerous interfaces for smart card, parallel and serial...

17/3,K/4 (Item 4 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

03456278 Supplier Number: 44822689 (USE FORMAT 7 FOR FULLTEXT)
UK leads multimedia for the masses
Electronics Times, p1
July 7, 1994
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 346

... digital satellite TV later this year, is also talking to Online about the technology.

The **set - top box** will use the ARM 610 **processor** with I/O and video **controller** chips also designed by ARM, an **MPEG** 1 image **decoder** from C-Cube, 2Mbyte of rom and at least 2Mbyte of ram. Online plans to...

17/3,K/5 (Item 1 from file: 696)
DIALOG(R)File 696:DIALOG Telecom. Newsletters

00665298
DTV set-top-on-a-chip from IBM Microelectronics will be
COMMUNICATIONS DAILY
April 14, 1999 DOCUMENT TYPE: NEWSLETTER
PUBLISHER: WARREN PUBLISHING INC.
LANGUAGE: ENGLISH WORD COUNT: 132 RECORD TYPE: FULLTEXT

TEXT:
...will enable programmers to offer new interactive, telephony and Internet services inexpensively through TV set. **STB** **controller** chip, announced Tues., combines PowerPC 401 **processor** , **MPEG** video **decoder** , onboard cache and memory, as well as numerous interfaces for smart card, parallel and serial...

...will enable programmers to offer new interactive, telephony and Internet services inexpensively through TV set. **STB** **controller** chip, announced Tues., combines PowerPC 401 **processor** , **MPEG** video **decoder** , onboard cache and memory, as well as numerous interfaces for smart card, parallel and serial...

22/3,K/1 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

07926399 Supplier Number: 65353124 (USE FORMAT 7 FOR FULLTEXT)
Controller IC Is Gateway To Multiple, Secure A/V. (Technology Information)
Grossman, Steve
Electronic Design, v48, n18, p86
Sept 5, 2000
Language: English Record Type: Fulltext Abstract
Document Type: Magazine/Journal; Trade
Word Count: 2628

... it can be enhanced even further for proprietary PVR systems.
A Plethora Of Buses
The **STB** /PVR controller IC has been configured with a **unified memory** architecture (UMA). This enables both the external **CPU** and the **STB** /PVR **controller** IC to share identical memory via the 32-bit SDRAM interface. The memory controller, which...

22/3,K/2 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

05232902 Supplier Number: 47979713 (USE FORMAT 7 FOR FULLTEXT)
Communications ICs: Nec pushes small offices to use ATM networks; ATM chip offers MPEG transfers
Lammers, David
Electronic Engineering Times, p57
Sept 15, 1997
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 427

... data directly from an ATM network to the MPEG decoder, reducing the load on the **CPU** .
The **controller** , the micron PD98409, **includes** an internal control **memory** for the 64 virtual channels used in **set - top - box** applications, removing the need for an external memory. It also supports a wide range of ...

22/3,K/3 (Item 1 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB

09756994 SUPPLIER NUMBER: 19781963 (USE FORMAT 7 OR 9 FOR FULL TEXT)
ATM chip offers MPEG transfers. (NEC's uPD98409 ATM segmentation and reassembly controller) (Product Announcement)
Lammers, David
Electronic Engineering Times, n971, p57(1)
Sep 15, 1997
DOCUMENT TYPE: Product Announcement ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext
WORD COUNT: 460 LINE COUNT: 00038

... data directly from an ATM network to the MPEG decoder, reducing the load on the **CPU** .

The **controller** , the micron PD98409, **includes** an internal control **memory** for the 64 virtual channels used in **set - top - box** applications, removing the need for an external memory. It also supports a wide range of ...

22/3,K/4 (Item 2 from file: 148)
DIALOG(R)File 148:Gale Group Trade & Industry DB
(c)2005 The Gale Group. All rts. reserv.

08675552 SUPPLIER NUMBER: 18293683 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Mitsubishi, NEC explore memory-MPU pairings. (Mitsubishi Electric's M32R/D microprocessor) (Product Announcement)
MacLellan, Andrew
Electronic News (1991), v42, n2116, p50(1)
May 13, 1996
DOCUMENT TYPE: Product Announcement ISSN: 1061-6624 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 775 LINE COUNT: 00064

...ABSTRACT: interested in exploring the possibility of reducing bus bandwidth tie-ups affecting multimedia applications by **integrating memory** on-chip with **microprocessor** functions. Mitsubishi unveiled its M32R/D **microprocessor** , designed for network **controller** , **set - top box** and personal digital assistant among other applications. The processor combines memory and CPU, along with...

22/3,K/5 (Item 1 from file: 647)
DIALOG(R)File 647:CMP Computer Fulltext
(c) 2005 CMP Media, LLC. All rts. reserv.

01138167 CMP ACCESSION NUMBER: EET19970915S0059
Communications ICs - Nec pushes small offices to use ATM networks - ATM chip offers MPEG transfers
David Lammers
ELECTRONIC ENGINEERING TIMES, 1997, n 971, PG57
PUBLICATION DATE: 970915
JOURNAL CODE: EET LANGUAGE: English
RECORD TYPE: Fulltext
SECTION HEADING: Design
WORD COUNT: 421

... data directly from an ATM network to the MPEG decoder, reducing the load on the **CPU** .
The **controller** , the micron PD98409, **includes** an internal control **memory** for the 64 virtual channels used in **set - top - box** applications, removing the need for an external memory. It also supports a wide range of...

```
File 348:EUROPEAN PATENTS 1978-2005/Jul W02
         (c) 2005 European Patent Office
File 349:PCT FULLTEXT 1979-2005/UB=20050714,UT=20050707
         (c) 2005 WIPO/Univentio

Set     Items   Description
S1       9195   STB OR SET()TOP()BOX OR SETTOP()BOX
S2       8243   STT OR SET()TOP()TERMINAL OR HCT OR HOME()COMMUNICATION()T-
             ERMINAL OR (CATV OR CABLE()TELEVISION OR CABLE OR SUBSCRIBER)-
             (3N)(BOX OR CONVERTER)
S3     262025   CPU OR CENTRAL()PROCESS?()UNIT OR PROCESSOR OR MICROPROCES-
             SOR OR MICRO()PROCESSOR
S4     195607   CONTROLLER OR MEMORY()CONTROLLER??
S5      91360   (UNIFIED OR INTEGRAT? OR COMBIN? OR INCLUD? OR JOIN? OR SI-
             NGL? OR ONE OR DISTINCT??)(3N)(MEMORY OR MEMORY()MODULE)
S6        257   AU=(LUNDBALD, J? OR LUNDBALD J? OR BALDWIN, J? OR BALDWIN -
             J? OR COFFIN, L? OR COFFIN L?)
S7        839   UMA OR UNIFIED()MEMORY()ARCHITECTURE
S8       3937   (EMBED? OR INCLUD?)(3N)BROWSER
S9       3235   (MPEG OR MOVING()PICTURE()EXPERT()GROUP)(3N)DECODER
S10     48483   S3(10N)S4
S11      2428   S10(10N)S5
S12         1   S11(10N)S1
S13         0   S11(10N)S2
S14         4   S11(10N)S7
S15         3   S14 NOT PY>2001
S16         0   S11(10N)S8
S17         0   S11(10N)S9
S18      8243   (S1 OR S2)(10N)S2
S19     24755   18(10N)S3
S20      2457   S19(10N)S4
S21        86   S20(10N)S5
S22         0   S21(10N)S7
S23         0   S21(10N)S8
S24         0   S21(10N)S9
S25        58   S21 NOT PY>2001
S26         1   S25 AND IC=H04N?
S27        58   IDPAT S25 (sorted in duplicate/non-duplicate order)
S28        56   IDPAT S25 (primary/non-duplicate records only)
S29        45   S28 NOT PD>010509
S30         0   S29 NOT (MAGNET OR HYDRAULIC OR FLUSHING OR POOL OR BANKNO-
             TE OR DISC OR SKEW OR NATIVE OR PLURALITY OR SCREEN OR PRINTER
              OR TAG OR ATOMIC OR FLOW OR POLARIZER OR RESISTANCE OR ELECT-
             ROGRAPHIC OR WHEEL OR DISPLAY OR SHARING OR CALLS OR REDUNDANT
              OR STACK OR
S31        18   S6 AND IC=H04N?
S32        10   S31 NOT PY>2001
S33        10   IDPAT (sorted in duplicate/non-duplicate order)
S34         7   IDPAT (primary/non-duplicate records only)
S35         0   S34(10N)(S1 OR S2)
S36         0   S35(10N)S3
S37         0   S35(10N)S4
S38         0   S35(10N)S5
S39         0   S35(10N)S7
S40         0   S35(10N)S8
S41         0   S35(10N)S9
```

12/3,K/1 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

01222234 **Image available**
BANKING VIDEO FRAMES ASSOCIATED WITH LINKS AND PROCESSING THE BANKED FRAMES ACCUMULATION ET TRAITEMENT DE TRAMES VIDEO ASSOCIEES A DES LIENS

Patent Applicant/Assignee:
AVANT INTERACTIVE INC, 1304 Carter Drive, Rockaway, NJ 07866, US, US (Residence), US (Nationality)
Inventor(s):
SALKIND Carole T, 1304 Carter Drive, Rockaway, NJ 07866, US,
FULCO William J, 1705 Pico Blvd., #121, Santa Monica, CA 90405, US,
SHIPP Michael S, 13935 West Tahiti, Way #248, Marina del Ray, CA 90292, US,
Legal Representative:
HOFFMAN David L (agent), Law Offices of David L. Hoffman, Suite 422, 27023 McBean Parkway, Valencia, CA 91355, US,
Patent and Priority Information (Country, Number, Date):
Patent: WO 200529453 A2 20050331 (WO 0529453)
Application: WO 2004US30674 20040916 (PCT/WO US04030674)
Priority Application: US 2003664350 20030916
Designated States:
(All protection types applied unless otherwise stated - for applications 2004+)
AE AG AL AM AT AU AZ BA BB BG BR BW BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NA NI NO NZ OM PG PH PL PT RO RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW
(EP) AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL PL PT RO SE SI SK TR
(OA) BF BJ CF CG CI CM GA GN GQ GW ML MR NE SN TD TG
(AP) BW GH GM KE LS MW MZ NA SD SL SZ TZ UG ZM ZW
(EA) AM AZ BY KG KZ MD RU TJ TM
Publication Language: English
Filing Language: English
Fulltext Word Count: 6644

Fulltext Availability:
Detailed Description

Detailed Description
... a user's or viewer's location, usually atop a TV/monitor 1 0. The **set top box** 8 normally, in the case of current PVR, has a **controller** or **CPU** 8a for performing the control functions, a **memory** 8b (which may **include** a PVR disk), and a converter 8c serving essentially as an input/output (1/0...

15/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00870100
HIGH PERFORMANCE UNIVERSAL MULTI-PORT INTERNALLY CACHED DYNAMIC RANDOM ACCESS MEMORY SYSTEM, ARCHITECTURE AND METHOD
SYSTEM, ARCHITEKTUR UND VERFAHREN MIT HOHER LEISTUNG FUR EINEN UNIVERSELLEN MULTIPORT DYNAMISCHEN DIREKTZUGRIFFSPEICHER MIT INTERNEM CACHE-SPEICHER
SYSTEME ET ARCHITECTURE DE MEMOIRE RAM DYNAMIQUE POLYVALENTE A CAPACITE ELEVEE POSSEDANT UNE ANTEMEMOIRE INTERNE ET DES ACCES MULTIPLES ET **PROCEDE**
PATENT ASSIGNEE:
Chatter, Mukesh, (2044140), 53 Godfrey Lane, Milford, Massachusetts 01757, (US), (Proprietor designated states: all)
INVENTOR:
Chatter, Mukesh, 53 Godfrey Lane, Milford, Massachusetts 01757, (US)
LEGAL REPRESENTATIVE:
Allsop, John Rowland (47689), MacLeod & Co., Bledington Grounds, Bledington, Gloucestershire OX7 6XL, (GB)
PATENT (CC, No, Kind, Date): EP 870303 A1 981014 (Basic)
EP 870303 B1 001018
WO 9724725 970710
APPLICATION (CC, No, Date): EP 96925929 960812; WO 96IB794 960812
PRIORITY (CC, No, Date): US 581467 951229
DESIGNATED STATES: AT; BE; CH; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; NL; PT; SE
INTERNATIONAL PATENT CLASS: G11C-007/00; G06F-013/16
NOTE:
No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	200042	1822
CLAIMS B	(German)	200042	1801
CLAIMS B	(French)	200042	2094
SPEC B	(English)	200042	8421
Total word count - document A			0
Total word count - document B			14138
Total word count - documents A + B			14138

...CLAIMS the control of parallel row internal transaction intervention means, thereby providing a chip suitable for **unified memory architecture** .
27. A system having a master **controller** such as **central processing unit** (**CPU**) having parallel data ports and a random access memory unit each connected to and competing...

15/3,K/2 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00385861 **Image available**
METHOD AND STRUCTURE FOR IMPROVING DISPLAY DATA BANDWIDTH IN A UNIFIED MEMORY ARCHITECTURE SYSTEM
PROCEDE ET STRUCTURE POUR AMELIORER LA LARGEUR DE BANDE DE DONNEES D'AFFICHAGE DANS UN SYSTEME D'ARCHITECTURE DE MEMOIRE UNIFIEE
Patent Applicant/Assignee:
MONOLOTHIC SYSTEM TECHNOLOGY INC,

Inventor(s):
HSU Fu-Chieh,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9726604 A1 19970724
Application: WO 97US14 19970115 (PCT/WO US9700014)
Priority Application: US 96379 19960116
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE HU IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK TJ TM TR TT UA UG UZ VN KE LS MW SD SZ UG AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 5331

Fulltext Availability:
Detailed Description

Detailed Description
... memory
architecture (UMA) computer system 300 in accordance with one embodiment of the present invention. **UmA** system includes **CPU** 301, system **controller** 302, data path **controller** 303, **unified** DRAM **memory** array 304, graphics controller 305, expansion frame buffer memory 306 and CRT display 307, Buses...memory 306.

The previously described interface signals are used to control the following operations within **UMA** system 300: (1) CPU 301 write to **unified memory** 304, (2) **CPU** 301 write to expansion frame buffer memory 306, (3) graphics **controller** 305 read from **unified memory** 304, (4) graphics **controller** 305 read from expansion frame buffer memory 306, (5) **CPU** 301 read from **unified memory** 304, and (6) CPU 301 read from expansion frame buffer memory 306. Each of these...

15/3,K/3 (Item 2 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00383982 **Image available**
HIGH PERFORMANCE UNIVERSAL MULTI-PORT INTERNALLY CACHED DYNAMIC RANDOM ACCESS MEMORY SYSTEM, ARCHITECTURE AND METHOD
SYSTEME ET ARCHITECTURE DE MEMOIRE RAM DYNAMIQUE POLYVALENTE A CAPACITE ELEVEE POSSEDANT UNE ANTEMEMOIRE INTERNE ET DES ACCES MULTIPLES ET PROCEDE
Patent Applicant/Assignee:
CHATTER Mukesh,
Inventor(s):
CHATTER Mukesh,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9724725 A1 19970710
Application: WO 96IB794 19960812 (PCT/WO IB9600794)
Priority Application: US 95581467 19951229
Designated States:
(Protection type is "patent" unless otherwise stated - for applications

prior to 2004)
AL AM AT AT AU AZ BB BG BR BY CA CH CN CU CZ CZ DE DE DK DK EE EE ES FI
FI GB GE HU IL IS JP KE KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX
NO NZ PL PT RO RU SD SE SG SI SK SK TJ TM TR TT UA UG US UZ VN KE LS MW
SD SZ UG AM AZ BY KG KZ MD RU TJ TM AT BE CH DE DK ES FI FR GB GR IE IT
LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 10570

Fulltext Availability:
Claims

Claim
... the control of parallel row internal transaction intervention means, thereby providing a chip suitable for **unified memory architecture** .

27 For use in a system having a master **controller** such as **central processing unit** (**CPU**) having parallel data ports and a random access memory unit each connected to and competing...

26/3,K/1 **(Item 1 from file: 349)**
DIALOG(R)File 349:PCT FULLTEXT

00467033 **Image available**
SIDEBOX DISPLAY CHANNEL LOOP CONTROLLER
UNITE DE COMMANDE DE BOUCLE DE CANAUX POUR AFFICHAGE DESIRE DE CANAUX
Patent Applicant/Assignee:
KEARNS Donovan E,
Inventor(s):
KEARNS Donovan E,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9857498 A1 19981217
Application: WO 98US8412 19980427 (PCT/WO US9808412)
Priority Application: US 97872626 19970610
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 11147
Main International Patent Class: **H04N-007/10**
International Patent Class: **H04N-007/14**
Fulltext Availability:
Detailed Description

Detailed Description
... 1 invention to include an input device I I for providing user inputs to the **controller** 10. **One** or more **memory** devices **18** may be associated with a **processor** 16 for storing infort-nation temporarily or permanently, as required. A display 20 may be controlled by the processor 16 through a display control 22.

In certain embodiments of the **controller** 10, the memory devices **18** may be physically included in a chip identified with the **processor** 16. In alternate embodiments, the memory device **18** may be connected to the **processor** 16 over a bus 19.

The memory device **18** may also **include** a read-only **memory** 76 (ROM), a random access memory 70 (RAM), and/or a non-volatile memory (NVRAM...

34/3,K/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00864204
DISPLAY SYSTEM
ANZEIGESYSTEM
SYSTEME D'AFFICHAGE
PATENT ASSIGNEE:
Digital Projection Limited, (2151171), Greenside Way, Middleton, Manchester M24 1XX, (GB), (applicant designated states: BE;DE;FR;GB)
INVENTOR:
BALDWIN, John, Lewis, Edwin , 65 Lakewood Road Chandlers Ford, Eastleigh Hampshire SO5 5AE, (GB)
BLAXTAN, Peter, William, 14B Oaklands Rise Welwyn, Hertfordshire AL6 0RN, (GB
LEGAL REPRESENTATIVE:
Beresford, Keith Denis Lewis et al (28273), BERESFORD & Co. 2-5 Warwick Court High Holborn, London WC1R 5DJ, (GB)
PATENT (CC, No, Kind, Date): EP 864110 A1 980916 (Basic)
WO 9720242 970605
APPLICATION (CC, No, Date): EP 96940022 961128; WO 96GB2948 961128
PRIORITY (CC, No, Date): GB 9524259 951128
DESIGNATED STATES: BE; DE; FR; GB
INTERNATIONAL PATENT CLASS: G02B-026/08; G09F-009/37; **H04N-009/31**
NOTE:
No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English

INVENTOR:
BALDWIN, John, Lewis, Edwin ...
...INTERNATIONAL PATENT CLASS: **H04N-009/31**

34/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00086107
DIGITAL TELEVISION TAPE RECORDING.
DIGITALE FERNSEHBANDAUFZEICHNUNG.
ENREGISTREMENT NUMERIQUE VIDEO SUR BANDE.
PATENT ASSIGNEE:
INDEPENDENT BROADCASTING AUTHORITY, (304390), 70 Brompton Road, London SW3 1EY, (GB), (applicant designated states: AT;DE;FR;GB)
INVENTOR:
BALDWIN, John Lewis Edwin , Cherwell 65 Lakewood Road, Chandlers Ford Eastleigh, Hampshire, (GB
LEGAL REPRESENTATIVE:
Crawford, Andrew Birkby et al (29761), A.A. THORNTON & CO. Northumberland House 303-306 High Holborn, London WC1V 7LE, (GB)
PATENT (CC, No, Kind, Date): EP 71618 A1 830216 (Basic)
EP 71618 B1 861008
WO 8202810 820819
APPLICATION (CC, No, Date): EP 82900376 820205; WO 82GB30
PRIORITY (CC, No, Date): GB 8103502 810205
DESIGNATED STATES: AT; DE; FR; GB
INTERNATIONAL PATENT CLASS: **H04N-005/92**
NOTE:
No A-document published by EPO

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS B	(English)	EPBBF1	669
CLAIMS B	(German)	EPBBF1	577
CLAIMS B	(French)	EPBBF1	737
SPEC B	(English)	EPBBF1	4278
Total word count - document A			0
Total word count - document B			6261
Total word count - documents A + B			6261

INVENTOR:
BALDWIN, John Lewis Edwin ...
INTERNATIONAL PATENT CLASS: **H04N-005/92**

34/3,K/3 (Item 3 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS
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00015999
PREDICTIVE DIFFERENTIAL PULSE-CODE MODULATION APPARATUS.
PRADIKTIVE DIFFERENZEN-PULSCODEMODULATIONS-VORRICHTUNG.
APPAREIL DE MODULATION DIFFERENTIELLE IMPULSION-CODE DE PREDICTION.
PATENT ASSIGNEE:
INDEPENDENT BROADCASTING AUTHORITY, 70 Brompton Road, London SW3, (GB),
(applicant designated states: DE;FR;GB)
INVENTOR:
BALDWIN, John Lewis Edwin , Cherwell 65 Lakewood Road Chandlersford,
Eastleigh Hampshire, (GB)
WILKINSON, James Hedley, 20 Valencia Way Andover, Hampshire, (GB
PATENT (CC, No, Kind, Date): EP 16048 A1 801001 (Basic)
WO 8000207 800207
APPLICATION (CC, No, Date): EP 79900675 790627; WO 79GB105 790627
PRIORITY (CC, No, Date): GB 7828071 780627
DESIGNATED STATES: DE; FR; GB
INTERNATIONAL PATENT CLASS: H04B-001/00; **H04N-007/12** ; **H04N-009/02**
NOTE:
No A-document published by EPO
LANGUAGE (Publication,Procedural,Application): English; English; English
INVENTOR:
BALDWIN, John Lewis Edwin ...
...INTERNATIONAL PATENT CLASS: **H04N-007/12 ...**

... **H04N-009/02**

34/3,K/4 (Item 4 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
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00353664 **Image available**
MULTIPLE SEQUENCE MPEG DECODER AND PROCESS FOR CONTROLLING SAME
DECODEUR MPEG A SEQUENCE MULTIPLE ET PROCESSUS DE COMMANDE
Patent Applicant/Assignee:
THE 3DO COMPANY,
Inventor(s):
WASSERMAN Steve C,
BALDWIN James Armand ,
MITSUOKA George

Patent and Priority Information (Country, Number, Date):
  Patent: WO 9636178 A1 19961114
  Application: WO 96US6510 19960508 (PCT/WO US9606510)
  Priority Application: US 95439085 19950510; US 95440464 19950510
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
  AL AM AT AU AZ BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU IS JP KE
  KG KP KR KZ LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE
  SG SI SK TJ TM TR TT UA UG UZ VN KE LS MW SD SZ UG AM AZ BY KG KZ MD RU
  TJ TM AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI
  CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 18262

Inventor(s):
... **BALDWIN James Armand**
Main International Patent Class: **H04N-007/12**

34/3,K/5 (Item 5 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2005 WIPO/Univentio. All rts. reserv.

00309818 **Image available**
DISPLAY DEVICE
DISPOSITIF D'AFFICHAGE
Patent Applicant/Assignee:
  RANK BRIMAR LIMITED,
Inventor(s):
  BALDWIN John Lewis Edwin ,
  ECKERSLEY Brian
Patent and Priority Information (Country, Number, Date):
  Patent: WO 9527970 A1 19951019
  Application: WO 94GB768 19940412 (PCT/WO GB9400768)
  Priority Application: WO 94GB768 19940412
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
  JP
Publication Language: English
Fulltext Word Count: 8704

Inventor(s):
  BALDWIN John Lewis Edwin ...
International Patent Class: **H04N-03:12**

34/3,K/6 (Item 6 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT
(c) 2005 WIPO/Univentio. All rts. reserv.

00261306 **Image available**
DISPLAY DEVICE
DISPOSITIF DE VISUALISATION
Patent Applicant/Assignee:
  RANK BRIMAR LIMITED,
  BALDWIN John Lewis Edwin,
  ECKERSLEY Brian,
Inventor(s):

BALDWIN John Lewis Edwin ,
ECKERSLEY Brian
Patent and Priority Information (Country, Number, Date):
Patent: WO 9409473 A1 19940428
Application: WO 93GB2129 19931014 (PCT/WO GB9302129)
Priority Application: GB 9221697 19921015; GB 9225675 19921209
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
GB US AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE
Publication Language: English
Fulltext Word Count: 8682
Inventor(s):
BALDWIN John Lewis Edwin ...
International Patent Class: **H04N-03:12**

34/3,K/7 (Item 7 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00185779
IMPROVEMENTS RELATING TO VIDEO SIGNAL PROCESSING
AMELIORATIONS RELATIVES AU TRAITEMENT DES SIGNAUX VIDEO
Patent Applicant/Assignee:
RANK CINTEL LIMITED,
BALDWIN John Lewis Edwin,
Inventor(s):
BALDWIN John Lewis Edwin
Patent and Priority Information (Country, Number, Date):
Patent: WO 9103122 A1 19910307
Application: WO 90GB1278 19900814 (PCT/WO GB9001278)
Priority Application: GB 8918560 19890815
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AT BE CH DE DK ES FR GB GB IT JP LU NL SE US
Publication Language: English
Fulltext Word Count: 5315

Inventor(s):
BALDWIN John Lewis Edwin ...
Main International Patent Class: **H04N-005/205**
International Patent Class: **H04N-05:202**